IN THE SPECIFICATION:

Paragraph beginning at line 17 of page 3 has been amended as follows:

First of all, since the contact hole 13 is formed so as to extend over the heavily doped source region 7 and the body contact region 8 when the contact hole 13 is formed, it is necessary to provide a large area of the contact hole 13 in consideration of a layout margin for deviation in alignment between both of the regions 7 and 8. In addition, in order to avoid electrical conduction between the gate electrode 6 and the source electrode 15, a space defined between the contact hole 13 and a pattern of the trench 4 needs to be set at intervals in consideration of the layout margin for deviation in alignment. Then, these settings become a cause for impeding scale down (shrink) of the vertical MOS transistor, and obstructs miniaturization, low cost promotion or enhancement of a driving ability.

Heading at line 8 of page 11 has been amended as follows:

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Paragraph beginning at line 4 of page 12 has been amended as follows:

A trench 4 is formed in a central portion of the surface of the source region 7, and a polycrystalline silicon gate electrode 6 is provided within the trench 4 through a gate insulating film 5. An upper surface of the polycrystalline silicon gate electrode 6 is made to coincide or agree with in level with an interface between the source region 7 and the body region 3. An intermediate insulating film is formed within a remaining portion of the trench above that level. Then, a source electrode 15 made of a metal film is formed on the main surface of the semiconductor substrate. The source region 7 and the body contact region 8 are electrically connected to each other through the source electrode 15. Here, ~~for~~ as the contact for the electrical connection, the silicon surface other than the silicon trench is uniformly exposed, and the metallic film 15 is made to flatly contact the semiconductor substrate.

Paragraph beginning at line 19 of page 15 has been amended as follows:

Next, B is implanted into the main surface of the semiconductor substrate in order to form a region 3 intended to become the body region of this vertical MOS transistor.

The semiconductor substrate is then subjected to the heat treatment to thereby form the P-type body region 3 which has an impurity concentration of $2e^{16}/cm^3$ to $2e^{17}/cm^3$ and has a depth of several μm to several tens of μm. Next, a portion of monocrystalline silicon corresponding to a region in which the trench is intended to be formed is exposed with an oxide film or a photo resist film as a mask, and silicon of the epitaxial layer 2 is selectively etched away across the body region 3 by utilizing the anisotropic etching method such as the RIE to form the trench 4.

Paragraph beginning at line 13 of page 18 has been amended as follows:

Next, the metal layer 15 for providing electric potentials for the source region 7 and the body region 3 is formed (refer to FIG. 10). In case of the related art example, there is adopted a method in which the contact hole is formed across the intermediate insulating film 9 so that the metal film selectively contacts only the heavily doped source region 7 and the heavily doped body region 8. In the present invention, however, since the heavily doped polycrystalline silicon 6 within the trench is covered with the intermediate insulating film 9, the metal contact can be attained with the metal film being formed over the transistor

region. In addition, since the substrate surface is previously planarized or flattened by utilizing the etch back method, the formed metal film also has high flatness (i.e., has a highly planar structure).

Paragraph beginning at line 20 of page 21 has been amended as follows:

As set forth hereinabove, according to the present invention, the miniaturization and high driving ability of the vertical MOS transistor can be attained. In addition, it is possible to provide ~~the~~ a highly reliable vertical MOS transistor, and it is also possible to realize ~~the~~ a low manufacturing cost due to shortening of the processes, reduction in the material cost, and enhancement of the yield.